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ROYAL SIGNALS & RADAR
ESTABLISHMENT

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SPECIFICATION OF VIPER2 IN Z

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PROCUREMENT EXECUTIVE,
MINISTRY OF DEFENCE,
RSRE MALVERN,
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Specification of Viper2 in Z

Author
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Date
October 1988

Summary

As a continuation of the use of the specification language Z which was used to specify the Viper1 microprocessor this paper covers the specification of the Viper2. This was completed before the definitive HOL specification was complete, therefore there is no proof of correspondence between the two. Using Z did highlight inconsistencies in the HOL specification that may not have appeared until later in the specification.

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1. Introduction

This Memorandum is a description of the proposed Viper2 microprocessor using the specification language Z. The description is a continuation of the work done on the Viper1 processor¹. This is a first attempt to specify the Viper2 and was done in parallel with the specification in Higher Order Logic (HOL)[†]. There may therefore be some inconsistencies between this document and the HOL description². Where this occurs the latter should be taken as the definitive description.

In safety critical applications it is necessary to ensure that continued operation or safe shutdown of a system is achieved when erroneous data is input. There are two methods to increase the integrity of a system: to analyse the software for errors and to use a processor that is known to be functionally correct. Further confidence is achieved by using multi-channel systems incorporating processors of dissimilar technologies but with the same functionality. The functionality of any device is determined by the designers specification. If an error exists in this then all the channels in the system will experience the same common mode error.


By using a number of different methods to specify a processor, errors that may be present in one specification may become apparent in another. This is most effective when the methods used are basically different in character. This can be completed by using proofs of correspondence to confirm that the two texts have the same meaning.

An expertise in the use of Z already exists at RSRE and by using a Z editor and type checker available on the Computing Divisions PerqFlex workstations the task of specifying Viper2 made a useful project for a vacation student, who already had a Knowledge of Z. As a guide to the strategy required for this description J. Bowan's Z specification of the M6800 microprocessor³ was used.

This report is the first attempt to specify the Viper2 in Z. It makes no attempt to explain the primary constructs of Z, nor to act as a tutorial in the use of Z to specify a microprocessor. Readers not familiar with Z should consult Specification Case studies⁴ edited by I. Hayes. Although the specification has been type checked, it has neither been proved equivalent to the HOL specification nor to be free from errors. Any inconsistencies or errors found in this document should be reported back to the Computing Division, RSRE.

[†]Higher Order Logic (HOL) is a design tool developed at the Cambridge Computing Laboratory.

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2 Basic Functions

2.1 Bits and Words

Bit $\in \{0,1\}$

Word $\in \{ w:N \rightarrow \text{Bit} \mid \#w > 0 \wedge \text{dom } w = 0 \dots (\#w) - 1 \}$

Bits are represented as the set of elements with values 0 or 1. Words are represented as a set of partial functions from natural numbers to Bits. The natural numbers correspond to the position of the bit in the word, ie the result of $w(n)$ (the word w acting on the value n) gives the $n+1^{\text{th}}$ Bit of the word w .

LSB,MSB : Word \rightarrow Bit

$\forall w : \text{Word} .$
LSB $w = w\ 0$
MSB $w = w\ \#w-1$

Find the most and least significant bits of the word.

val : Word \rightarrow N

$\forall w : \text{Word} .$
 $(\#w=1) \Rightarrow (\text{val } w = \text{LSB } w)$
 $(\#w>1) \Rightarrow (\text{val } w = \text{LSB } w + 2 * \text{val}(\text{succ } w))$

val returns the natural number represented by the word. Note $\text{succ } w$ gives the effect of a Right shift, ie divide by two, on the word. ie if $\text{succ } w$ is applied to n then first $\text{succ } n$ is calculated, and then w of $n+1$ is calculated ie the $n+2^{\text{th}}$ Bit is returned rather than the $n+1^{\text{th}}$ one.

pred : $N_1 \rightarrow$ N

$\forall n : N . \text{pred } n = n - 1$

Useful for left shifting (in a similar way to the technique described above).

(_set_) : (Word*Bit) \rightarrow Word

$\forall w : \text{Word}; b : \text{Bit} .$
 $w \text{ set } b = w \setminus ((0wb).(1wb))$

The set function returns a word which has all of its bits set to the specified value.

maxval : Word \rightarrow N

$\forall w : \text{Word} .$
maxval $w = \text{val}(w \text{ set } 1)$

$$\vdash (\exists w : \text{Word} . ((\text{val } w) > \text{maxval } w))$$

Returns the maximum value which can be stored in the word.

$\text{wrd} : N_1 \rightarrow (N \rightarrow \text{Word})$	$\vdash \text{size} : N_1 ; \text{valu} : N ; w : \text{Word} .$ $(\text{wrd } \text{size } \text{valu} = w) \Leftrightarrow$ $((\#w = \text{size}) \wedge$ $(\text{val } w = \text{valu mod succ}(\text{maxval } w)))$
--	---

The function wrd returns the word of size size and set to the value valu (if that value can be held in a word of that size). Note no algorithm is given for calculating wrd from its arguments, just the relationships which must hold between the word returned and the input arguments.

$(_ \wedge _) : (\text{Word} * \text{Word}) \rightarrow \text{Word}$	$\vdash w1, w2 : \text{Word} .$ $w1 \wedge w2 = w1 \cup (\text{pred } \#w1 ; w2)$
--	---

$$\vdash w1, w2 : \text{Word} . \#(w1 \wedge w2) = \#w1 + \#w2$$

Concatenate two words together.

2.2 Bitwise Functions

not : Bit → Bit

not = {0→1,1→0}

Generate the logical inverse of the input bit.

(_+_),(_+_),(+_): (Bit→Bit)→Bit

(_+_)	= {(0,0)→0,(0,1)→1,(1,0)→1,(1,1)→1}
-------	-------------------------------------

(_+_)	= {(0,0)→0,(0,1)→1,(1,0)→1,(1,1)→0}
-------	-------------------------------------

(_+_)	= {(0,0)→0,(0,1)→0,(1,0)→0,(1,1)→1}
-------	-------------------------------------

Standard bitwise logical functions. (note + is exclusive or)

Viper_aux_1 keeps ..+,+,not,*,wrd,maxval,set,pred,val,LSB,MSB,
Word,Bit

2.3 Logical functions on words

$w_{\text{not}} : \text{Word} \rightarrow \text{Word}$	$\forall w : \text{Word} .$ $w_{\text{not}} w = w ; \text{not}$
--	--

Generate the inverse of the input word.

WordPair \triangleq
 $\{ w : \mathbb{N} \rightarrow (\text{Bit} \rightarrow \text{Bit}) \mid \#w > 0 \wedge \text{dom } w = 0 \dots ((\#w)-1) \}$

$(_ \text{pair} _) : (\text{Word} \times \text{Word}) \rightarrow \text{WordPair}$	$\forall w_1, w_2 : \text{Word} .$ $w_1 \text{ pair } w_2 =$ $\{ i : \mathbb{N} \mid i \in \text{dom } w_1 \cap \text{dom } w_2 \rightarrow i \mapsto (w_1 i, w_2 i) \}$
--	--

Takes a pair of words and represents them as a set of bit pairs, indexed by a single natural number.

$(_ \text{and} _), (_ \text{or} _), (_ \text{exor} _) : (\text{Word} \times \text{Word}) \rightarrow \text{Word}$	$\forall w_1, w_2 : \text{Word} .$ $w_1 \text{ and } w_2 = ((w_1 \text{ pair } w_2) ; (_ \text{and} _))$ $w_1 \text{ or } w_2 = ((w_1 \text{ pair } w_2) ; (_ \text{or} _))$ $w_1 \text{ exor } w_2 = ((w_1 \text{ pair } w_2) ; (_ \text{exor} _))$
---	---

Standard wordwise logical functions.

$(_ \ll _) : (\text{Word} \times \text{Bit}) \rightarrow \text{Word}$	$\forall w : \text{Word}; b : \text{Bit} .$ $w \ll b = (\{ \#w \} \triangleleft (\text{pred } \#w)) \cup \{ 0 \mapsto b \}$
---	--

$(_ \gg _) : (\text{Bit} \times \text{Word}) \rightarrow \text{Word}$	$\forall w : \text{Word}; b : \text{Bit} .$ $b \gg w = \{ ((\#w)-1) \mapsto b \} \cup (\text{succ } \#w)$
---	--

Shift right and left while inserting a particular bit into the right or left most position.

2.4 Arithmetic Functions

```

value : Word → ℤ

ℳ w : Word →
  ((MSB w = 1) ∧ value w = val w - succ (maxval w)) ∨
  ((MSB w = 0) ∧ value w = val w)

```

Return the integer value represented by the Word. This is using the 2's complement notation. (Remember the most significant bit has a weighting of -2^{n-1} . So to cope with negative numbers subtract 2^n).

```

maxpos, maxneg : Word → ℤ
|
∀ w1, w2 : Word | #w1 = ((#w2)+1) .
    maxpos w1 = maxval w2
    maxneg w1 = (maxval w2) - (maxval w1)

```

Return the maximum positive and negative numbers for a word of a particular size.

```

(_s.signextend_) : (Word = N1) → Word

```

```

∀ w1, w2 : Word : length : N1 |
    (length ≥ #w1) ∧ (#w2 = length) .
    (w1.signextend length) = (w2.set (MSB w1)) • w1

```

Sign extends the word to the length specified.

$$\begin{aligned} &(\text{_pad_}) : (\text{Word} = N_1) \rightarrow \text{Word} \\ &\forall w_1, w_2 : \text{Word}; \text{length} : N_1 \mid \\ &\quad (\text{length} \geq \#w_1) \wedge (\#w_2 = \text{length}) . \\ &(\text{w1 pad length}) = (w_2 \text{ set } 0) \bullet w_1 \end{aligned}$$

Pad out a word to the new word length with zeros

$$w \text{ trim length} = (0 \dots \text{length}) \triangleleft w$$

Trim a word down to the new word length. Note, use the above with caution, as it simply returns a word with the top bits 'trimmed' off. No check is made to ensure that the value of the word has not changed.

```
(_plus_) : (Word*Word) → Word
```

```

∀ w1,w2,w3 : Word | (#w1) = ((#w2)+1) ∧ (#w2) = (#w3) .
  (w2 plus w3 = (w1 trim #w2))
    ⇔ (value w1) = (value w2) + (value w3)

```

The word returned by plus is the same size as the two input words, and holds the value of the sum of the two words, iff this value can be held in a word of that size.

```
(_times_) : (Word*Word) → Word
```

```

∀ w1,w2,w3 : Word | (#w1) = ((#w2)*2) ∧ (#w2) = (#w3) .
  (w2 times w3 = (w1 trim #w2))
    ⇔ (value w1) = (value w2) * (value w3)

```

The word returned by times is the same size as the two input words, and holds the value of the product of the two words, iff this value can be held in a word of that size.

```
(_minus_) : (Word*Word) → Word
```

```

∀ w1,w2,w3 : Word | (#w1) = ((#w2)+1) ∧ (#w2) = (#w3) .
  (w2 minus w3 = (w1 trim #w2))
    ⇔ (value w1) = (value w2) - (value w3)

```

The word returned by minus is the same size as the two input words, and holds the value of the difference of the two words, iff this value can be held in a word of that size.

```
(_carry_) : (Word*Word) → Bit
```

```

∀ w1,w2 : Word .
  (w1 carry w2 = 1) ⇔ ((val w1) + (val w2) > maxval w1)

```

Top level specification of carry, ie a carry is generated when the result is larger than the maximum possible value which can be stored.

```
(_mcarry_) : (Word*Word) → Bit
```

```

∀ w1,w2 : Word .
  (w1 mcarry w2 = 1) ⇔ ((val w1) + (val w2) > maxval w1)

```

Top level specification of carry for multiplication.

```
(_borrow_) : (Word*Word) → Bit
```

```

∀ w1,w2 : Word .
  (w1 borrow w2 = 1) ⇔ ((val w1) < (val w2))

```

Top level specification of Borrow.

```

| (_overflow_) : (Word*Word) → Bit
|-----
  ∀ w1,w2 : Word | #w1 = #w2 .
    (w1 overflow w2 = 1) ⇔
      ( ( (value w1) + (value w2) > maxpos w1 ) ∨
        ( (value w1) + (value w2) < maxneg w2 ) )

```

Top level specification of overflow, ie overflow when the sum is greater than the largest positive value which can be held, or less than the largest negative number.

```

| (_moverflow_) : (Word*Word) → Bit
|-----
  ∀ w1,w2 : Word | #w1 = #w2 .
    (w1 moverflow w2 = 1) ⇔
      ( ( (value w1) + (value w2) > maxpos w1 ) ∨
        ( (value w1) + (value w2) < maxneg w2 ) )

```

Top level specification of overflow for multiplication.

```

| (_underflow_) : (Word*Word) → Bit
|-----
  ∀ w1,w2 : Word | #w1 = #w2 .
    (w1 underflow w2 = 1) ⇔
      ( ( (value w1) - (value w2) > maxpos w1 ) ∨
        ( (value w1) - (value w2) < maxneg w2 ) )

```

Top level specification of overflow on subtraction.

```

| (_equal_) : (Word*Word) → Bit
|-----
  ∀ w1,w2 : Word | #w1 = #w2 .
    (w1 equal w2 = 1) ⇔ (val w1 = val w2)

```

Returns 1 if the two numbers are the same.

```

| (_less_) : (Word*Word) → Bit
|-----
  ∀ w1,w2 : Word | #w1 = #w2 .
    (w1 less w2 = 1) ⇔ (value w1 < value w2)

```

Returns 1 if the first number is less than the second.

This completes the underlying theory of representing natural number arithmetic by operations on vectors of bits.

3 Viper Specifics

3.1 Word Lengths

```
Word64 = { w : Word | #w = 64 }
Word32 = { w : Word | #w = 32 } -- For Double length integers
-- For Data words
Word20 = { w : Word | #w = 20 }
-- For Address words
Word4 = { w : Word | #w = 4 }
-- For the function select
Word3 = { w : Word | #w = 3 }
-- For the destination select
Word2 = { w : Word | #w = 2 }
-- For the register and memory
-- select
Word1 = { w : Word | #w = 1 }
-- For the comparison select
-- and flags
```

Address = Word20

Data = Word32

Flag = Word1

Values
one.zero : Word
True.False : Flag
value zero = 0
value one = 1
True = {0~1}
False = {0~0}

3.2 Memory

The definition of the memory and peripheral spaces, and the behaviour of these two regions.

Memory	
Mem	: Address \rightarrow Data
PERIspace	: Address \rightarrow Data
RAMspace	: Address \rightarrow Data
io	: Bit
$(io = 0) \Rightarrow (Mem = RAMspace)$ $(io = 1) \Rightarrow (Mem = PERIspace)$	

If io is zero then all memory reads are from the RAM space. If io is one then all of the reads are from the PERIspace.

Δ Memory	
Memory	
Memory'	
ΔMem	: Address \rightarrow Data
$(io = 0) \Rightarrow (RAMspace' = RAMspace \oplus \Delta Mem)$ $(io = 1) \Rightarrow (RAMspace' = RAMspace)$	

If io is zero then any writes will affect the value in the memory, if however io is one there are no changes to RAM. Note changes to PERI are not modeled.

\exists Memory	
Δ Memory	
ΔMem	= 0

No change in memory.

3.3 Registers

The specification of the Viper2 registers.

[RegName]

Register $a \{ r: \text{RegName} \rightarrow \text{Word} \mid \#r > 0 \}$

The Registers are the partial function from Register names to Words.

$\text{Reg} : \text{RegName} \rightarrow \text{Word}$ $\forall n : \text{RegName}; \text{Regs} : \text{Register} .$ $\text{Reg } n = \text{Regs } n$
--

Returns the value in the Register given as input.

GeneralPurposeRegisters	
A, X, Y, Z1, Double : RegName	
Reg A	$\in \text{Word}_{32}$
Reg X	$\in \text{Word}_{32}$
Reg Y	$\in \text{Word}_{32}$
Reg Z1	$\in \text{Word}_{32}$
Reg Double	$\in \text{Word}_{64}$
Reg Double	$= (\text{Reg } A) \wedge (\text{Reg } Z1)$

The four general purpose read write registers (note X, Y, Z1 are index registers. The register double is the concatenation of the A and Z registers.

AddressRegisters	
F, S, U, P : RegName	
Reg F	$\in \text{Word}_{20}$
Reg S	$\in \text{Word}_{20}$
Reg U	$\in \text{Word}_{20}$
Reg P	$\in \text{Word}_{20}$

The four addressing registers. The Frame pointer F points to the start of the current stack frame. The Frame size S is the size of the current stack frame (ie the stack frame goes from F to F+S). The stack Limit U is the furthest up the stack is allowed to grow. Finally The Program Counter P is the position in memory where the current instruction was read from.

OtherRegisters

D.Watchdog.Temp : RegName

Reg D € Word₃₂

Reg Watchdog € Word₃₂

Reg Temp € Word₃₂

The three remaining registers. The D register is the error message register. If an error occurs then the error code for that particular error is placed in D. The Watchdog register is used when operating in untrusted mode. The value in Watchdog is the number of clock cycles left to complete any untrusted operations. The registers Temp hold the next 32-bit instruction to be executed.

ProcessFlags

B.Postcall.Trust : RegName

Reg B € Word₁

Reg Postcall € Word₁

Reg Trust € Word₁

The three process flags are held as one bit registers. The B flag contains the result from various comparisons or unsigned arithmetic. The Postcall flag is there to ensure that the Enter instruction always occurs after a call instruction, and never anywhere else. It is set true after a call and cleared during an enter. The Trust flag determines whether the machine is in trusted or untrusted mode.

ErrorFlags

E,IA,IX,IY,IZ,IB,WE,NoStack,NoSize,NoLimit : RegName

Reg E € Word₁

Reg IA € Word₁

Reg IX € Word₁

Reg IY € Word₁

Reg IZ € Word₁

Reg IB € Word₁

Reg WE € Word₁

Reg NoStack € Word₁

Reg NoSize € Word₁

Reg NoLimit € Word₁

The error flags. The E flag is set true if there has been an error. This is utilised by the Jump on error and Call on error instructions. The IA, IX, IY, IZ and IB flags show whether a register holds an invalid value, ie IA is true if A has not been loaded since the machine started, or since an error occurred. The WE register is set if the Watchdog timer has Expired (hence WE). This flag will cause an

error to occur if it is set while the machine is in untrusted mode. It is ignored in trusted mode. The NoStack, NoSize and NoLimit Flags are set true if the F, S and U registers have not been set.

```

Regs & ErrorFlags A
ProcessFlags A
OtherRegisters A
AddressRegisters A
GeneralPurposeRegisters

```

The Viper2 register types

```

registers
Regs
Registers : Register

```

The registers at split time consist of a 'bank' of registers and the Viper2 register types.

```

ΔRegisters
registers
registers'
newp      : Address
NewWatchdog : Data
NewWE     : Flag
ΔReg      : RegName → Word

Registers' = Registers • {Pnewp, WE → NewWE}
              • {Watchdog → NewWatchdog} • ΔReg

```

The Viper2 registers. The new values of the registers are the same as the old value, apart from the three registers which are always updated (the program counter, watchdog timer and watchdog expired flag). These can be overwritten by any modifications to them in ΔReg. Any other changes in the registers (due to the various instructions) are also contained in ΔReg.

```

ΣRegisters
ΔRegisters
ΔReg = {}

```

All of the registers remain the same (apart from the three above)

3.4 Clock

The Viper2 clock is not represented in the HDL specification.
A definition is included here for completeness.

Clock
Clk : N

Clock simply counts up from 0.

Δ Clock
Clock
Clock'
Cycles : N
$Clk' = Clk + Cycles$

Cycles is the number of cycles needed to complete the present instruction. The parameter cycles is used by the Watchdog timer.

3.5 Stop

The definition of the Stop Flag.

Stop
stop : Bit

The single bit to determine whether the machine is stopped or not.

Δ Stop
Δ Registers
Stop
Stop'
Values
sval : Bit
stop = 0
newp = Reg (P) plus one

The machine has not stopped. The new value of the Program Counter is P+1. The value of stop' is set later in the specification.

3.6 Viper State

Δ State Δ Memory A
 Δ Registers A
 Δ Clock A
 Δ Stop

The Viper2 changing state. The change in the Viper state is the change in memory and the change in registers and the change in stop.

ArithmeticAndLogicalUnit	
r,m	: Data
offs	: Data
base	: Data
Result	: Data

The inputs and outputs to/from the ALU. r and m are the two inputs to the ALU and Result is the result from it. Base is the base address to read the memory (m) input to the ALU from and offs is the actual address of the read.

3.7 Viper2 Operation Codes

Viper2OpCode	
op	: Word ₃₂
s1	: Word ₂
s2	: Word ₄
s2l	: Word ₂
s2u	: Word ₂
fq	: Word ₂
fc	: Word ₄
fc1	: Word ₂
fch	: Word ₂
addr	: Word ₂₀
$op = s2 \wedge s1 \wedge fq \wedge fc \wedge addr$ $fc = fch \wedge fc1$ $s2 = s2u \wedge s2l$	

The Viper2 Op code. Op is the op code and is loaded from the address pointed to by the Program Counter. The op code is the concatenation of the five fields shown: s2, s1, fq, fc and addr. The fc and s2 fields are further subdivided into two 2 bit fields.

The s2 field selects the addressing mode for the m input to the ALU if the instruction is a data operation, or whether the operation is a control or write instruction. The s1 field selects the register (r) input to the ALU or the type of certain load instructions. The fq (functional qualifier) field selects the destination register of the data instructions, or whether the instruction is a control or a write instruction. It also determines the type of call or branch performed (ie absolute or Program Counter relative). The fc (function code) determines the instruction to be performed. Finally the addr field determines the location to jump to, write to, read from etc.

3.8 Viper2 Overall State

```

Viper2Inputs
attention : Bit
reset     : Bit

```

The two external input lines. These are assumed to be synchronous lines clocked in at the start of each instruction. The attention line is set by external devices to inform the processor when they require attention. It is polled by the Jump and Call on attention instructions.

```

ΔViper2
ΔState
ArithmeticAndLogicalUnit
Viper2OpCode
Viper2Inputs
Values

op  = Mem (Reg (P))
reset = 0
(Reg WE = False) ⇒ (NewWatchdog=(Reg Watchdog)
                    minus (wrd 32 Cycles))
(NewWE = True) ⇒ ((Reg Watchdog) borrow (wrd 32 Cycles) = 1)

```

The op code is the value in the memory location pointed to by Program Counter. The reset line must be low, otherwise the machine will reset. The new value of the Watchdog Expired flag will be set to True if the watchdog counter will become less than zero in the course of the present instruction (not quite true as WE in fact goes true immediately the Watchdog timer goes below zero). The watchdog timer is decremented if the WE flag is not set.

```

Stopped
EMemory
ERegisters
Stop
Stop'
ΔClock

stop = 1
stop' = 1
newp = Reg (P)

```

The machine has stopped, and cannot restart until there is a Reset.

```

EViper2
ΔViper2
EMemory
ERegisters
ΔStop

```

Viper state unchanged (except P, Watchdog and WE updated)

Reset EMemory ΔRegisters ΔClock ΔStop Viper2Inputs Values
stop' = 0 reset = 1 val newp = 0 ΔReg = {E=False, IA=True, IX=True, NoStack=True, NoSize=True, IY=True, IZ=True, IB=True, Trust=True, NoLimit=True, WE=False, Watchdog=((Reg Watchdog) set 1)}

Machine status on a Reset. All of the Register Illegal flags are set to true (as the registers have not had any values loaded into them yet). The error flag is set false, as is the Watchdog Expired flag. The program counter is set to zero.

Viper2INIT Reset Clk' = 0

Machine on start up.

Viper2_machine_state keeps

ΔClock, Stop, ΔStop, ΔViper2, EViper2, Viper2INIT,
ΔMemory, EMemory, registers, ΔRegisters, Clock,
Address, Data, Flag, Memory, Reset, Reg, Word₆₄,
Word₃₂, Word₂₀, Word₄, Word₃, Word₂, Word₁, Stopped,
RegName

This section specifies the inputs to the Viper2 ALU.

invalid : Word → Bit w : Word * (invalid w = 1) ⇔ (val w > maxval (wrd 20 0))

Returns True if the value is greater than can be held in a 20 bit word.

ErrorInstruction

ΔViper2

ErrorValue : Data

The instruction being executed is illegal. The error code of the particular error is returned in ErrorValue.

IllegalP

ErrorInstruction

val (Reg P) = maxval (Reg P)

(val s2 = 15) v (val fq = 3) v (val fc ≥ 7)

The program counter is about to carry, and the current instruction is not a jump. (there is no need to cause an error if the instruction is a jump, as there is no 'return' as in a call instruction).

4 Viper Operations

4.1 Viper2 ALU

This section specifies the vi input to the Viper2 ALU

RegisterSelect	
$\Delta Viper2$	
<hr/>	
(val s1 = 0) \Rightarrow (r = Reg A)	
(val s1 = 1) \Rightarrow (r = Reg X)	
(val s1 = 2) \Rightarrow (r = Reg Y)	
(val s1 = 3) \Rightarrow (r = Reg Z1)	

Select the register to be used as the r input to the ALU.

DataInstruction	
$\Delta Viper2$	
<hr/>	
val s2 = 15	

The instruction is a data instruction. If s2 was 15 then it would be a control or write instruction.

4.2 Addressing Modes

```
GlobalAddressing _____  
DataInstruction _____  
val s2u = 0  
Reg Trust = True  
base = addr pad 32
```

Relative addressing mode. The base address is the address in the Op code. The machine must be in trusted mode.

```
StackRelativeAddressing _____  
DataInstruction _____  
val s2u = 1  
base = (addr pad 32) plus (Reg F pad 32)
```

Stack relative addressing. This gives access to local routine variables. The base address is the frame pointer offset by the address from the Op code. No check is made here to see if the address calculated is in the current stack frame. This is done in a later error frame.

```
ProgramCounterRelativeAddressing _____  
DataInstruction _____  
val s2u = 2  
base = (addr pad 32) plus (Reg P pad 32)
```

Program Counter relative addressing. This gives access to constants embedded in the program. This allows routines to be relocatable in memory (ie standard ROMs can be bought which can plug straight into a system). The base address is the program counter plus the input address.

```
AddressBases = GlobalAddressing v StackRelativeAddressing  
              v ProgramCounterRelativeAddressing
```

The three basic addressing modes. The base address is offset by the various index registers (or not in the case of absolute addressing).

```
AbsoluteAddressing _____  
AddressBases _____  
val s2l = 0  
offs = base
```

Absolute Addressing. The location to read in from is simply the base address defined above.


```

XIndexedAddressing _____
AddressBases
val s21 = 1
offs    = base plus (Reg X)

```

Indexed Addressing using the X index register. The location to read in from is the base address plus the value contained in the X index register. Note the value in X can be either a positive or a negative value. This can be used to index arrays etc.

```

YIndexedAddressing _____
AddressBases
val s21 = 2
offs    = base plus (Reg Y)

```

Indexed Addressing using the Y index register. The location to read in from is the base address plus the value contained in the Y index register. Note the value in Y can be either a positive or a negative value. This can be used to index arrays etc.

```

ZIndexedAddressing _____
AddressBases
val s21 = 3
offs    = base plus (Reg Z)

```

Indexed Addressing using the Z index register. The location to read in from is the base address plus the value contained in the Z index register. Note the value in Z can be either a positive or a negative value. This can be used to index arrays etc.

```

IndexedAddressing & ZIndexedAddressing v YIndexedAddressing
v AbsoluteAddressing v XIndexedAddressing

```

All of the simple addressing modes.

```

IndexAddressing _____
IndexedAddressing
val fc = 13
val s2 = 12
m = Mem (offs trim 20)
io = 0

```

The simple addressing modes. This does not include the case of the monadic instructions, where a memory read will not be taking place, or the Immediate and Register addressing modes, where no memory read is taking place. The value on the io pin is zero, so the word read in is read from the RAM space. The m input to the ALU is the value in the location pointed to by offset. The case of offset being outside the 20 bit address space is dealt with in the errors later.

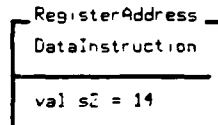
ImmediateAddressing _____

DataInstruction _____

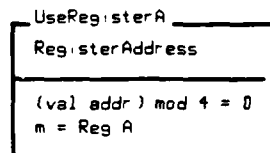
(val s2 = 12)^(m = addr pad 32) v
(val s2 = 13)^(m = wnot (addr pad 32))

The two Immediate Addressing modes. The m input to the ALU is the value in the address field padded with zeros to 32 bits, if s2 is 12. If s2 is 13 then the m input is this value inverted (ie 1's complement). This allows both negative and positive values to be used as constants.

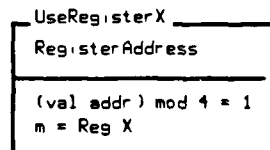
4.3 Access to General Purpose Registers



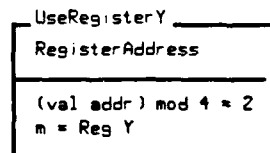
In this case the m input to the ALU is one of the general purpose registers A, X, Y, or Z. Which register is used is determined by the bottom two bits in the address field of the op code.



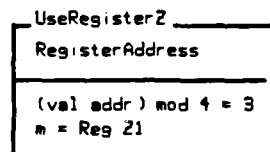
The A register is used as the m input to the ALU.



The X register is used as the m input to the ALU.



The Y register is used as the m input to the ALU.



The Z register is used as the m input to the ALU.

RegisterAddressing = UseRegisterA v UseRegisterX
v UseRegisterY v UseRegisterZ

The four cases of register addressing.

MemoryRead = ImmediateAddressing v IndexAddressing
v RegisterAddressing

The fifteen cases of memory addressing for the fifteen values sZ can have for any data instruction.

4.4 Illegal Addressing Operations

StackNotSet	
DataInstruction	
ErrorInstruction	
<hr/>	
val s2u = 1	
Reg NoStack = True	
deltaMem = {}	

Stack Relative addressing has been specified, however no stack has been set up (ie no value has been loaded into F).

UnsetX	
AddressBases	
ErrorInstruction	
<hr/>	
val s2l = 1	
Reg IX = True	
deltaMem = {}	

The X register has been selected as the index register to be used, but it has either not been loaded, or an error has occurred in untrusted mode and all of the registers have been marked as illegal

UnsetY	
AddressBases	
ErrorInstruction	
<hr/>	
val s2l = 2	
Reg IY = True	
deltaMem = {}	

The Y register has been selected as the index register to be used, but it has either not been loaded, or an error has occurred in untrusted mode and all of the registers have been marked as illegal

UnsetZ	
AddressBases	
ErrorInstruction	
<hr/>	
val s2l = 3	
Reg IZ = True	
deltaMem = {}	

The Z register has been selected as the index register to be used, but it has either not been loaded, or an error has occurred in untrusted mode and all of the registers have been marked as illegal

```
UnsetAddressingRegister & StackNotSet
  v UnsetZ
  v UnsetY
  v UnsetX
```

The four cases of illegally used registers.

IllegalStackAddress

IndexedAddressing
ErrorInstruction

```
val fc ≠ 13
val s2u = 1
((val offs) < (val (Reg F))) ∨
 (val offs) > (val (Reg F)) + (val (Reg S)))
ΔMem = {}
```

IllegalReadAddress

IndexedAddressing
ErrorInstruction

```
val fc ≠ 13
val s2 < 12
invalid offs = 1
ΔMem = {}
```

This is the only check that is needed to see if the address is valid. This is because the base address is at most a 21 bit number, so there can be no overflow on the first addition. The index register added to this base value can be one of four cases.

(1) The index register holds a +ve number and the result causes overflow. Then the MSB of result is one and hence above predicate detects the invalid address.

(2) The index register holds a +ve number and no overflow occurs. Then the address is valid iff the above predicate holds.

(3) The index register holds a -ve number and a carry occurs. Then the result must be a positive number less than the base. It is valid.

(4) The index register is negative and no carry occurs, ie the index register held a negative number which was 'larger' than the base. This is detected as for -ve numbers MSB = 1, and hence invalid address.

The case of -ve index register and overflow cannot occur as base is ALWAYS positive.

4.5 Illegal Source Registers

RegisterAInvalid
RegisterAddress
ErrorInstruction
(val addr) mod 4 = 0
Reg IA = True
δMem = {}

Register addressing has been specified, with the *m* input to the ALU coming from the A register. This register however does not contain valid data.

RegisterXInvalid
RegisterAddress
ErrorInstruction
(val addr) mod 4 = 1
Reg IX = True
δMem = {}

Register addressing has been specified, with the *m* input to the ALU coming from the X register. This register however does not contain valid data.

RegisterYInvalid
RegisterAddress
ErrorInstruction
(val addr) mod 4 = 2
Reg IY = True
δMem = {}

Register addressing has been specified, with the *m* input to the ALU coming from the Y register. This register however does not contain valid data.

RegisterZInvalid
RegisterAddress
ErrorInstruction
(val addr) mod 4 = 3
Reg IZ = True
δMem = {}

Register addressing has been specified, with the *m* input to the ALU coming from the Z register. This register however does not contain valid data.

RegisterInvalid & RegisterAInvalid v RegisterXInvalid
v RegisterYInvalid v RegisterZInvalid

The four cases where an illegal register has been selected to be the m input to the ALU.

```

RegisterSelectInvalidError _____
ΔViper2
ErrorInstruction
_____
( (val s2 = 15 ∧ val fc = 13 ) ∨
  (val fq = 3 ∧ val fc < 12 ) ∨
  (val fc = 6 ) )
ΔMem = {}

```

The instruction selected requires a register be the r input to the ALU. (ie either a dyadic data instruction s2 = 15 and fc = 13, a write instruction s2 = 15, fq = 3 and fc < 12 (this last condition because fc ≥ 12 would give a different error code), or the instruction is decrement with branch on zero.

```

RegisterSelectAInvalid _____
RegisterSelectInvalidError
_____
val s1 = 0
Reg IA = True

```

The instruction requires the r input to the ALU to be the A register, but this register does not contain valid data.

```

RegisterSelectXInvalid _____
RegisterSelectInvalidError
_____
val s1 = 1
Reg IX = True

```

The instruction requires the r input to the ALU to be the X register, but this register does not contain valid data.

```

RegisterSelectYInvalid _____
RegisterSelectInvalidError
_____
val s1 = 2
Reg IY = True

```

The instruction requires the r input to the ALU to be the Y register, but this register does not contain valid data.

```

RegisterSelectZInvalid _____
RegisterSelectInvalidError
_____
val s1 = 3
Reg IZ = True

```

The instruction requires the r input to the ALU to be the Z register, but this register does not contain valid data.

RegisterSelectInvalid ▲ RegisterSelectZInvalid
▼ RegisterSelectYInvalid
▼ RegisterSelectXInvalid
▼ RegisterSelectAInvalid

The four cases of illegal register being used for the r input to the ALU.

4.6 Comparison Operations

CompareFrame
RegisterSelect
MemoryRead
Bresult : Word ₁
ΔMem = {}

Framing schema for comparison operations. All registers are unchanged except for the Program counter. B is set in the various comparisons below.

GreaterThanOrEqualTo
CompareFrame
val fc = 0
Bresult = wrd 1 (not (r less m))

Bresult is set true if the r input is greater than or equal to the m input.

EqualTo
CompareFrame
val fc = 1
Bresult = wrd 1 (r equal m)

Bresult is set true if the r input is equal to the m input.

GreaterThan
CompareFrame
val fc = 2
Bresult = wrd 1 (not((r less m) + (r equal m)))

Bresult is set true if the r input is greater than the m input.

UnsignedLessThan
CompareFrame
val fc = 3
Bresult = wrd 1 (r borrow m)

Bresult is set true if the r input, treated as an unsigned integer, is less than the m input.

```

AndEqualZero _____
CompareFrame
_____
val fc = 4
Bresult = wrd 1 ((r and m) equal (zero))

```

Bresult is set true if the r input logically anded with the m input is equal to zero.

```

CompOp = AndEqualZero v UnsignedLessThan v GreaterThan
        v EqualTo v GreaterThanOrEqualTo

```

The five basic comparison operations. B is loaded with the following

```

Condition _____
CompOp
_____
val fq = 0
δReg = {B←Bresult, IB←False}

```

B is loaded with Bresult. The Illegal B flag is set false to show that the B register contains valid information.

```

NotCondition _____
CompOp
_____
val fq = 1
δReg = {B←wnot(Bresult), IB←False}

```

B is loaded with not Bresult. The Illegal B flag is set false to show that the B register contains valid information.

```

BorCondition _____
CompOp
_____
val fq = 2
δReg = {B←( Reg(B) or Bresult ), IB←False}

```

B is loaded with Bresult or B. The Illegal B flag is set false to show that the B register contains valid information.

```

BorNotCondition _____
CompOp
_____
val fq = 3
δReg = {B←( Reg (B) or wnot(Bresult) ), IB←False}

```

B is loaded with not Bresult or B. The Illegal B flag is set false to show that the B register contains valid information.

```

Compare = Condition v BorNotCondition
          v BorCondition v NotCondition

```

The four operations loading B with a result. There are $15 \times 4 \times 20 = 1200$ compare operations out of the possible 2^{12} Viper2 operations.

4.7 Viper2 Arithmetic

ALUInstruction
RegisterSelect
MemoryRead
$\delta B : \text{RegName} \leftrightarrow \text{Word}$
$\delta \text{Mem} = \{\}$

Framing schema for all of the ALU operations. Note memory cannot be changed. δB holds any changes to the B register.

SignedAdd
ALUInstruction
$\text{val fc} = 5$
$\text{Result} = r \text{ plus } m$
$\delta B = \{\}$

Add r to m. There is no check for overflow, this is done later in an error schema.

UnsignedAdd
ALUInstruction
$\text{val fc} = 6$
$\text{Result} = r \text{ plus } m$
$\delta B = \{\text{B} \leftarrow \text{word } 1 (r \text{ carry } m), \text{IB} \leftarrow \text{false}\}$

Add r to m, setting B if there is a Carry. IB is set false whatever the result.

SignedSubtract
ALUInstruction
$\text{val fc} = 7$
$\text{Result} = r \text{ minus } m$
$\delta B = \{\}$

Subtract r from m. There is no check for underflow, this is done later in an error schema.

```

UnsignedSubtract _____
ALUInstruction
_____
val fc = 8
Result = r minus m
ΔB     = {Borrow 1 (r borrow m), IB=False}

```

Subtract m from r, and setting B if there is a Borrow. IB is set false whatever the result.

```

SignedMultiply _____
ALUInstruction
_____
val fc = 12
Result = r times m
ΔB     = {}

```

Multiply r by m. There is no check for overflow, this is done later in an error schema.

```

ArithmeticOp & ( UnsignedAdd v SignedSubtract v SignedMultiply
                  v UnsignedSubtract v SignedAdd )

```

The five arithmetic operations. There are $15 \times 4 \times 5 = 300$ possible operations (ie 15 addressing modes by four register inputs by five possible operations).

4.8 Logical Operations

ExclusiveOr
ALUInstruction
val fc = 11
Result = r exor m
dB = {}

Returns the exclusive or of the two input words.

And
ALUInstruction
val fc = 9
Result = r and m
dB = {}

Returns the logical and of the two inputs.

Or
ALUInstruction
val fc = 10
Result = r or m
dB = {}

Returns the logical or of the two inputs.

LogicalOp = (Or v And v ExclusiveOr)

The three logical operators. There are $15 \times 4 \times 3 = 180$ possible logical operations.

4.9 Load Instruction

```

MonadicInstruction
  IndexedAddressing
   $\delta B : \text{RegName} \leftrightarrow \text{Word}$ 

  val fc = 13
  
```

The operation is a monadic or load instruction. There is no register select, the only operand comes from the m input to the ALU. The register select field s1 is used to determine which operation is performed.

```

LoadRegister
  MonadicInstruction

  val s1 = 0
  Result = Mem(off s trim 20)
   $\delta B = \{\}$ 
  io = 0
  
```

Simply load the register with a value from a memory location.

```

LoadAndNegateRegister
  MonadicInstruction

  val s1 = 1
  Result = zero minus (Mem(off s trim 20))
   $\delta B = \{\}$ 
  io = 0
  
```

Load and find the 2's complement of the value from a memory location. There is no check to see if there has been an overflow as this is done in a later error schema.

```

LoadEffectiveAddress
  MonadicInstruction

  val s1 = 2
  Result = offs
   $\delta B = \{\}$ 
  val s2 = 12
  io = 0
  
```

Load the address determined by the addressing mode into the result.

InputFromPERI
Monad.cInstruction
val s1 = 3
Result = Mem(offst 20)
dB = {}
val s2 = 3
io = 1

Load in a word from PERIpheral space.

LoadOp = LoadRegister v LoadAndNegateRegister
v LoadEffectiveAddress v InputFromPERI

One of the four load operations. There are $15 \times 1 \times 4 = 60$ possible operations.

ALU = LogicalOp v ArithmeticOp v LoadOp

An ALU operation. At present there are $300 + 180 + 60 = 540$ operations defined.

4.10 Destination Registers

```
ResultToA _____  
ALU  
-----  
val fq = 0  
δReg  = {A←Result, IA←False} • δB
```

Load the result from the ALU into the A register and set the IA flag false to show that there is valid data in the A register. Also set the B and IB flags if they should be set by this operation.

```
ResultToX _____  
ALU  
-----  
val fq = 1  
δReg  = {X←Result, IX←False} • δB
```

Load the result from the ALU into the X register and set the IX flag false to show that there is valid data in the X register. Also set the B and IB flags if they should be set by this operation.

```
ResultToY _____  
ALU  
-----  
val fq = 2  
δReg  = {Y←Result, IY←False} • δB
```

Load the result from the ALU into the Y register and set the IY flag false to show that there is valid data in the Y register. Also set the B and IB flags if they should be set by this operation.

```
ResultToZ1 _____  
ALU  
-----  
val fq = 3  
δReg  = {Z1←Result, IZ1←False} • δB
```

Load the result from the ALU into the Z1 register and set the IZ1 flag false to show that there is valid data in the Z1 register. Also set the B and IB flags if they should be set by this operation.

$ALUDp \bullet ResultToA \vee ResultToX \vee ResultToY \vee ResultToZ1$

Load one of the four general purpose registers. There are $540 = 4 \times 2160$ possible operations. The two other function codes $fc = 13$, $fc = 14$ will give another $15 \times 4 \times 2 \times 4 = 480$ operations. This means that in total there are 2640 data operations possible.

4.11 Exception Handling for ALU Operations

```
SignedAddOverflow _  
ALUInstruction  
ErrorInstruction  
  
val fc = 5  
(r overflow m) = 1  
δMem = {}
```

An overflow has occurred on a signed add.

```
SignedSubtractUnderflow _  
ALUInstruction  
ErrorInstruction  
  
val fc = 7  
(r underflow m) = 1  
δMem = {}
```

An underflow has occurred on a signed subtract.

```
SignedMultiplyOverflow _  
ALUInstruction  
ErrorInstruction  
  
val fc = 12  
(r overflow m) = 1  
δMem = {}
```

An overflow has occurred on a signed multiply.

```
LoadAndNegateRegisterOverflow _  
MonadicInstruction  
ErrorInstruction  
  
val s1 = 1  
m = Mem(offset trim 20)  
(zero underflow m) = 1  
δMem = {}
```

An underflow has occurred when loading and negating a register. This means that the value which was loaded must have been maxneg.

```

LoadEffectiveAddressError
  MonadInstruction
  ErrorInstruction
  -----
  val s1 = 2
  val s2 > 12
  δMem = {}

```

Illegal operation, if $s2 > 12$ then it is immediate or register addressing, ie there is no 'effective address'.

```

InputFromPERIError
  MonadInstruction
  ErrorInstruction
  -----
  val s1 = 3
  val s2 > 3
  δMem = {}

```

The operation is an input from PERI, but the addressing mode is not global.

```

IllegalAddress
  MonadInstruction
  ErrorInstruction
  -----
  val s1 = 2
  invalid offs = 1
  δMem = {}

```

The operation has been defined as a load address but the address is not legal.

```

MonError = LoadEffectiveAddressError ∨
          InputFromPERIError

```

```

MonadError = MonError ∨
             ~ (MonError) ∧ IllegalAddress

```

```

MonadError = MonadError ∨
             ~ (MonadError) ∧ LoadAndNegateRegisterOverflow

```

Needed to cope with two errors in the same instruction. A load Effective Address Error will be noticed before an Illegal Input Address error which will be noticed before a Load and negate register overflow.

```

ArithError = SignedAddOverflow ∨
             SignedSubtractUnderflow ∨
             SignedMultiplyOverflow ∨
             MonadError

```

The Errors which can occur during ALU operations.

4.12 Jumps and Calls

```
ControlInstruction
MemoryRead

val s2 = 15
val fq = 3
```

The instruction is a control instruction.

```
DestinationSelect
ControlInstruction
Destination : Word32

(val fq = 0)A(Destination = addr pad 32)
      v
(val fq = 1)A
(Destination = (addr pad 32) plus (newp pad 32))
      v
(val fq = 2)A
(Destination = (addr pad 32) minus (newp pad 32))
```

The framing schema for a jump or a call. Destination is the location to call or branch to. Note three types of jump, absolute or Program Counter relative forwards or backwards.

```
UnconditionalJump
DestinationSelect

val fc = 0
δReg = {P←(Destination trim 20)}
δMem = {}
```

Unconditional jump. P is loaded with the value of destination.

```
JumpIfError
DestinationSelect

val fc = 1
Reg Trust = True
val (Reg E) = 1
δReg = {P←(Destination trim 20),IA←False,
        IX←False,IY←False,IZ←False,IB←False}
δMem = {}
```

Jump if the E (error) flag is set. Set all of the Illegal Register flags to false?

JumpIfBSet
DestinationSelect
val fc = 2 val (Reg B) = 1 δReg = {Pw(Destination trim 20)} δMem = {}

Jump if the B flag is set.

JumpIfBNotSet
DestinationSelect
val fc = 3 val (Reg B) = 0 δReg = {Pw(Destination trim 20)} δMem = {}

Jump if the B flag is not set.

JumpIfAttentionSet
DestinationSelect
val fc = 4 attention = 1 δReg = {Pw(Destination trim 20)} δMem = {}

Jump if the attention input to the Viper2 microprocessor is set.

JumpIfAttentionNotSet
DestinationSelect
val fc = 5 attention = 0 δReg = {Pw(Destination trim 20)} δMem = {}

Jump if the attention input to the Viper2 microprocessor is not set.

FailedJumpCondition
ControlInstruction
EViper2
((val fc = 1) A (val (Reg E) = 0)) v ((val fc = 2) A (val (Reg B) = 0)) v ((val fc = 3) A (val (Reg B) = 1)) v ((val fc = 4) A (attention = 0)) v ((val fc = 5) A (attention = 1))

If the Jump condition is false, then Viper2 state the same (apart from the Program counter increment).

```
DecrementAndJumpOnNotZero
DestinationSelect
RegisterSelect
δPC : RegName → Data

val fc = 6
Result = r minus one
(Result ≠ zero) ⇒ (δPC = {P←(Destination trim 20)})
(Result = zero) ⇒ (δPC = {})
(val s1 = 0) ⇒ (δReg = {A←Result, I←False} • δPC)
(val s1 = 1) ⇒ (δReg = {X←Result, IX←False} • δPC)
(val s1 = 2) ⇒ (δReg = {Y←Result, IY←False} • δPC)
(val s1 = 3) ⇒ (δReg = {Z1←Result, IZ←False} • δPC)
δMem = {}
```

Decrement the selected register, and jump if it is not zero.

```
CallInstruction
DestinationSelect
δFlags : RegName → Data
TopOfCallFrame, BottomOfNewWorkspace : Data
BottomOfCallFrame, ProgramStatusWord : Data

BottomOfCallFrame = ((Reg F) pad 32) plus
                    ((Reg S) pad 32)
TopOfCallFrame = BottomOfCallFrame plus one
ProgramStatusWord = (Reg P) pad 32 • (20←val(Reg Trust))
BottomOfNewWorkspace = TopOfCallFrame plus one

δMem = {(BottomOfCallFrame trim 20)←(Reg F),
        (TopOfCallFrame trim 20)←(ProgramStatusWord)}
δReg = {F←(BottomOfNewWorkspace),
        P←(Destination trim 20), Postcall←True}
        • δFlags
```

The Call instruction. Set up the link frame on the stack, set the frame pointer to point to the bottom of the new workspace, set the postcall register to True to ensure that the next instruction is an Enter and load in the new value for the program counter. The value in the error flags may also alter if there is a call on Error instruction. The link frame consists of two data words.

The first word is placed in the location above the top of the previous stack frame and is loaded with the old frame pointer. The second word is placed in the location above the first word. This holds the return program counter as well as the old value of the trust bit.

```
UnconditionalCall
CallInstruction

val fc = 8
δFlags = {}
```

Unconditional jump. P is loaded with the value of destination.

```
CallIfError _____  
CallInstruction  
  
val fc = 9  
val (Reg E) = 1  
δFlags = {IA=False,IX=False,IY=False,  
          IZ=False,IB=False,E=False}
```

Call if the E (error) flag is set. Set all of the Illegal Register flags to false?

```
CallIfBSet _____  
CallInstruction  
  
val fc = 10  
val (Reg B) = 1  
δFlags = {}
```

Call if the B flag is set.

```
CallIfBNotSet _____  
CallInstruction  
  
val fc = 11  
val (Reg B) = 0  
δFlags = {}
```

Call if the B flag is not set.

```
CallIfAttentionSet _____  
CallInstruction  
  
val fc = 12  
attention = 1  
δFlags = {}
```

Call if the attention input to the Viper2 microprocessor is set.

```
CallIfAttentionNotSet _____  
CallInstruction  
  
val fc = 13  
attention = 0  
δFlags = {}
```

Call if the attention input to the Viper2 microprocessor is not set.

FailedCallCondition	
ControlInstruction	
EUiper2	
((val fc = 9) ^ (val (Res E) = 0))	v
((val fc = 10) ^ (val (Res B) = 0))	v
((val fc = 11) ^ (val (Res B) = 1))	v
((val fc = 12) ^ (attention = 0))	v
((val fc = 13) ^ (attention = 1))	

If the Call condition is false, then Viper2 state the same (apart from the Program counter increment).

4.13 Copy Instruction

CopyFromRegisterToGeneralPurposeRegister

ControlInstruction

ad : N

```
val fc = 7
val fq = 0
ad = (val addr) mod 16
(ad = 0) => (Result = Reg A)
(ad = 1) => (Result = Reg X)
(ad = 2) => (Result = Reg Y)
(ad = 3) => (Result = Reg Z1)
(ad = 4) => (Result = (Reg P) pad 32)
(ad = 5) => (Result = (Reg F) pad 32)
(ad = 6) => (Result = (Reg S) pad 32)
(ad = 7) => (Result = (Reg U) pad 32)
(ad = 8) => (Result = (Reg Watchdog) pad 32)
(ad = 9) => (Result = Reg D)
```

Copy from a register to a general purpose register.

CopyToGeneralPurposeRegister

CopyFromRegisterToGeneralPurposeRegister

```
(val s1 = 0) => (dReg = {A←Result,IA←False})
(val s1 = 1) => (dReg = {X←Result,IX←False})
(val s1 = 2) => (dReg = {Y←Result,IY←False})
(val s1 = 3) => (dReg = {Z1←Result,IZ←False})
```

Place value in general purpose register.

CopyFromGeneralPurposeRegisterToRegister

ControlInstruction

RegisterSelect

ad : N

```
val fc = 7
val fq = 1
Reg Trust = True
ad = (val addr) mod 16
(ad = 0) => (dReg = {A←r,IA←False})
(ad = 1) => (dReg = {X←r,IX←False})
(ad = 2) => (dReg = {Y←r,IY←False})
(ad = 3) => (dReg = {Z1←r,IZ←False})
(ad = 4) => (dReg = {P←(r trim 20)})
(ad = 5) => (dReg = {F←(r trim 20),NoLimit←True,
                    NoSize←True,NoStack←False})
(ad = 6) => (dReg = {S←(r trim 20),NoSize←False})
(ad = 7) => (dReg = {U←(r trim 20),NoLimit←False})
(ad = 8) => (dReg = {Watchdog←(r trim 16),WE←False})
(ad = 9) => (dReg = {D←r})
```

Copy a value from a general purpose register to a special register.

4.14 Enter and Return

Enter
ControlInstruction
<pre> val fc = 14 (val (Reg F)) + (val addr) + 2 ≤ (val (Reg U)) Reg Postcall = True (val fq = 0) ⇒ (δReg = {Swaddr, Postcall ← False}) (val fq = 1) ⇒ (δReg = {Swaddr, Trust ← False, Postcall ← False}) (val fq = 2) ⇒ (δReg = {Swaddr, Trust ← True, Postcall ← False}) </pre>

The Enter Instruction. This must be executed immediately after a call instruction. If it is called at any other time it will generate an error. The enter instruction sets up the frame size required by the routine, after checking that at least 2 words of memory are free at the top of the new frame to accomodate a call instruction in the new routine. It also sets up the trusted ness of the routine. Finally the postcall bit is reset.

Return
CallInstruction
<pre> TopOfCallFrame = (Reg F) minus one ProgramStatusWord = Mem(TopOfCallFrame) BottomOfCallFrame = TopOfCallFrame minus one BottomOfNewWorkspace = Mem(BottomOfCallFrame) δReg = {F ← (BottomOfNewWorkspace), P ← (ProgramStatusWord trim 20), T ← (ProgramStatusWord 20), S ← (BottomOfCallFrame minus (BottomOfNewWorkspace trim 20))} </pre>

The Return from subroutine command. This basically undoes the call command. The frame pointer (F) program counter and trust bit are reloaded from the link frame. The value in the frame size register is calculated and loaded back in.

Copies CopyFromGeneralPurposeRegisterToRegister v
 CopyToGeneralPurposeRegister

The two copy commands. This covers $1 \times 4 \times 1 \times 2 = 8$ operations.

Jump UnconditionalJump v JumpIfError v
 JumpIfAttentionSet v JumpIfBNotSet v
 DecrementAndJumpOnNotZero v JumpIfAttentionNotSet v
 JumpIfBSet

Jumps Jump v FailedJumpCondition

The seven jump commands. This covers $1 \times 4 \times 7 \times 3 = 84$ operations.

Call * UnconditionalCall v CallIfError v
CallIfBSet v CallIfBNotSet v CallIfAttentionSet v
CallIfAttentionNotSet

Calls * Call v FailedCallCondition

The six call commands. This covers $1 \times 4 \times 6 \times 3 = 72$ operations.

Control * Calls v Jumps v Copies v Enter v Return

The control operations. There are $8 + 84 + 72 + 1 \times 4 \times 2 \times 3 = 188$ operations.

4.14 Illegal Calls and Jumps

```

IllegalJump _____
Jump
ErrorInstruction
_____
invalid Destination = 1

```

The operation is a jump but the destination is not in memory space.

```
IllegalJumpCondition _____
Jumps
ErrorInstruction
Reg IB = True
(val fc = 2) v (val fc = 3)
```

The jump is dependant on B, but B has not been set.

```
IllegalJumps  ▲ IllegalJump  ▼
                IllegalJumpCondition
```

```

IllegalCallError
ControlInstruction
ErrorInstruction
DestinationSelect
TopOfCallFrame, BottomOfNewWorkspace : Data
BottomOfCallFrame, ProgramStatusWord : Data

(val fc ≥ 8) ∧ (val fc ≤ 13)
BottomOfCallFrame      = ((Reg F) pad 32) plus
                        ((Reg 5) pad 32)
TopOfCallFrame         = BottomOfCallFrame plus one
ProgramStatusWord      = (Reg P) pad 32 ♦ (20→val(Reg Trust))
BottomOfNewWorkspace   = TopOfCallFrame plus one

```

Framing schema for Call errors.

```

IllegalDestination
IllegalCallError

invalid Destination = 1
deltaMem = {}

```

The operation is a call but the destination is not in memory space.

```

IllegalBottomOfCallFrame _____
IllegalCallError
invalid BottomOfCallFrame = 1
δMem    = {}

```

The bottom of the call space is not in memory.

```

IllegalTopOfCallFrame _____
IllegalCallError
invalid TopOfCallFrame = 1
δMem    = {(BottomOfCallFrame trim 20)⌘(Reg F)}

```

The top of the call space is not in memory. This is only noticed after the first write to memory has been made.

```

IllegalBottomOfNewWorkspace _____
IllegalCallError
invalid BottomOfNewWorkspace = 1
δMem    = {(BottomOfCallFrame trim 20)⌘(Reg F),
           (TopOfCallFrame trim 20)⌘(ProgramStatusWord)}

```

The bottom of the new work space is not in memory. This is only noticed after the first two writes to memory have been made.

```

StackNotSet _____
IllegalCallError
(Reg NoStack = True) ∨ (Reg NoSize = True)
δMem    = {}

```

A call has been made with the stack not set.

```

IllegalCalls * IllegalDestination      ∨
              IllegalBottomOfCallFrame ∨
              IllegalTopOfCallFrame    ∨
              IllegalBottomOfNewWorkspace ∨
              StackNotSet

```

All of the Illegal Call schemas.

4.15 Illegal Copy

CopyError1

ControlInstruction
ErrorInstruction

```
val fc = 7
val fq = 0
deltaMem = {}
((val addr = 0) ^ (Reg IA = True)      v
 (val addr = 1) ^ (Reg IX = True)      v
 (val addr = 2) ^ (Reg IY = True)      v
 (val addr = 3) ^ (Reg IZ = True)      v
 (val addr = 5) ^ (Reg NoStack = True) v
 (val addr = 6) ^ (Reg NoSize = True)  v
 (val addr = 7) ^ (Reg NoLimit = True) )
```

Attempt to copy invalid register.

CopyError2

ControlInstruction
ErrorInstruction

```
val fc = 7
val fq = 1
Reg Trust = True
deltaMem = {}
((val s1 = 0) ^ (Reg IA = True) v
 (val s1 = 1) ^ (Reg IX = True) v
 (val s1 = 2) ^ (Reg IY = True) v
 (val s1 = 3) ^ (Reg IZ = True) )
```

Attempt to copy invalid register.

IllegalCopy

ControlInstruction
ErrorInstruction

```
val fc = 7
val fq = 1
Reg Trust = False
deltaMem = {}
```

Attempt to copy to protected register, in untrusted mode.

IllegalCopies = CopyError1 v CopyError2 v IllegalCopy

Error in copying from register to register.

LimitNotSet
ControlInstruction
ErrorInstruction
val fc = 14
deltaMem = {}

Limit is not set in enter instruction.

4.16 Postcall and Enter Errors

PostcallNotSet

ControlInstruction
ErrorInstruction

val fc = 14
Reg Postcall = False
δMem = {}

Postcall is not set and Enter has been found, ie Enter has occurred somewhere other than at the start of a subroutine.

EnterNotFound

ControlInstruction
ErrorInstruction

val fc = 14
Reg Postcall = True
δMem = {}

Postcall is set and Enter has not been found, ie Enter has not occurred at the start of a subroutine.

StackOverflow

ControlInstruction
ErrorInstruction

val fc = 14
(val (Reg F)) + (val addr) + 2 > (val (Reg U))
Reg Postcall = True
δMem = {}

The stack cannot accomodate the present frame.

4.17 Write Operations

```
WriteInstruction
RegisterSelect

val s2 = 15
val fq = 3
val fc = 11
δReg = {}
```

Write instruction. Note $fc > 11$ is an illegal op code.

```
GlobalWrite
WriteInstruction

val fch = 0
base = addr pad 32
io = 0
Reg Trust = True
```

Write to Global memory.

```
LocalStackFrameWrite
WriteInstruction

val fch = 1
base = (addr pad 32) plus (Reg F)
io = 0
```

Write to local stack frame.

```
OutputToPERI
WriteInstruction

val fch = 2
base = addr pad 32
io = 1
```

Output to PERIpheral.

WriteBase \vee GlobalWrite \vee LocalStackFrameWrite \vee OutputToPERI

The three addressing modes.

```
Write
WriteBase

(val fcl = 0  $\wedge$  offs = base  $\vee$ 
 val fcl = 1  $\wedge$  offs = base plus (Reg X)  $\vee$ 
 val fcl = 2  $\wedge$  offs = base plus (Reg Y)  $\vee$ 
 val fcl = 3  $\wedge$  offs = base plus (Reg Z1) )
δMem = {(offs trim 20)  $\rightarrow$  r}
```

Write to the location specified. Either absolute addressing or indexed addressing. Write has $1 \times 4 \times 1 \times 12 = 48$ Operations.

4.18 Write Errors

```

WriteError
WriteInstruction
ErrorInstruction

(val fcl = 0) ^ (offs = base) v
(val fcl = 1) ^ (offs = base plus (Reg X)) v
(val fcl = 2) ^ (offs = base plus (Reg Y)) v
(val fcl = 3) ^ (offs = base plus (Reg Z)) v

```

Write error framing schema.

```

IllegalIndex
WriteInstruction
ErrorInstruction

(val fcl = 1) ^ (Reg IX = True) v
(val fcl = 2) ^ (Reg IY = True) v
(val fcl = 3) ^ (Reg IZ = True) v

```

The index register specified is illegal.

```

GlobalWriteError
WriteError

val fch = 0
δMem = {}
invalid offs = 1

```

The write location is not in the memory space.

```

StackFrameWriteError
WriteError

val fch = 1
δMem = {}
( invalid offs = 1
  (val offs) < (val (Reg F)) v
  (val offs) > (val (Reg F)) + (val (Reg S)) ) v

```

The write location is not in the stack frame.

```

GlobalOutputError
WriteError

val fch = 2
δMem = {}
invalid offs = 1

```

The output location is not in the memory space.

IllegalWriteAddress * GlobalWriteError v
StackFrameWriteError v
GlobalOutputError v
IllegalIndex

The Write Errors.

4.19 Other Viper2 Errors

```

WatchdogTimeout
ΔViper2
ErrorInstruction

Reg WE = True
Reg Trust = False

```

The watchdog timer has timed out, and Viper2 is in untrusted mode.

```

IllegalOpCode
ΔViper2
ErrorInstruction

val s2 = 15
((val fc = 6) ∧ (val fq = 2)) ∨
((val fq = 3) ∧ (val fc ≥ 12))

```

An illegal Op code. There are $1 \times 4 \times 1 \times 1 + 1 \times 4 \times 1 \times 4 = 20$ possibilities.

```

Viper2_Error ≡ IllegalP
UnsetAddressingRegister
RegisterSelectInvalid
RegisterInvalid
IllegalReadAddress
ArithError
IllegalJumps
IllegalCopies
LimitNotSet
EnterNotFound
StackOverflow
PostcallNotSet
IllegalCalls
IllegalWriteAddress
WatchdogTimeout
IllegalOpCode

```

The Viper2 Error conditions.

```

arb : Word → Word

∀ w1, w2 : Word | w1 = w2 ⇒ w1 = arb w2

```

The arb function, ie no relationship between input and output words

```

TrustedError
Viper2_Error

Reg Trust = True
stop' = 1

```

Error in trusted state, machine stops.

```

UntrustedError
Viper2_Error
CallInstruction

Reg Trust = False
TopOfCallFrame      = (Reg F) minus one
ProgramStatusWord   = Mem(TopOfCallFrame)
BottomOfCallFrame   = TopOfCallFrame minus one
BottomOfNewWorkspace = Mem(BottomOfCallFrame)
δReg = {A←(arb (Reg A)),IA←True,
        X←(arb (Reg X)),IX←True,
        Y←(arb (Reg Y)),IY←True,
        Z1←(arb (Reg Z1)),IZ←True,
        B←(arb (Reg B)),IB←True,
        E←True,
        F←(BottomOfNewWorkspace),
        P←(ProgramStatusWord trim 20),
        Trust←(ProgramStatusWord 20),
        S←(BottomOfCallFrame minus
            (BottomOfNewWorkspace trim 20))}

stop' = 0

```

Error in untrusted state. Set all Error falgs true and return from subroutine.

Viper2_Errors = UntrustedError ∨ TrustedError

4.20 The Viper Top Level Specification

NotStopped
Δ Viper2
stop' = 0

ViperOK \triangleq Compare \vee ALUOp \vee Control \vee Write

Viper2 has successfully completed an operation. There are $1200 + 2640 + 188 + 48 + 20 = 4096$ possible operations, ie all Op codes accounted for.

OKState $\triangleq \neg(\text{Viper2_Errors}) \wedge \text{ViperOK} \wedge \text{NotStopped}$

NextState $\triangleq \text{Viper2_Errors} \vee \text{OKState} \vee \text{Stopped} \vee \text{Reset}$

The next state of the Viper2 machine.

5 Conclusions

This document gives an initial specification of the Viper2 in Z. It has been shown that Z provides a higher level of specification than that written in HOL. It has also demonstrated that it is a useful language to produce a high level specification of a microprocessor.

This specification was completed before the HOL specification was complete and so no attempt was made to ensure conformity between the two.

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7 References

1. Kemp D.H. Specification of Viper1 in Z
2. Cullyer W.J. Viper2 Microprocessor: Formal Specification
 To be published.
3. Bowen J. The Formal Specification of a Microprocessor
 Instruction Set.
4. Hayes I. (editor) Specification Case Studies
 Prentice-Hall International series in
 computer science, 1987.

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Abstract As a continuation of the use of the specification language Z which was used to specify the Viper 1 microprocessor this paper covers the specification of the Viper 2. This was completed before the definitive HOL specification was complete, therefore there is no proof of correspondence between the two. Using Z did highlight inconsistencies in the HOL specification that may not have appeared until later in the specification.				